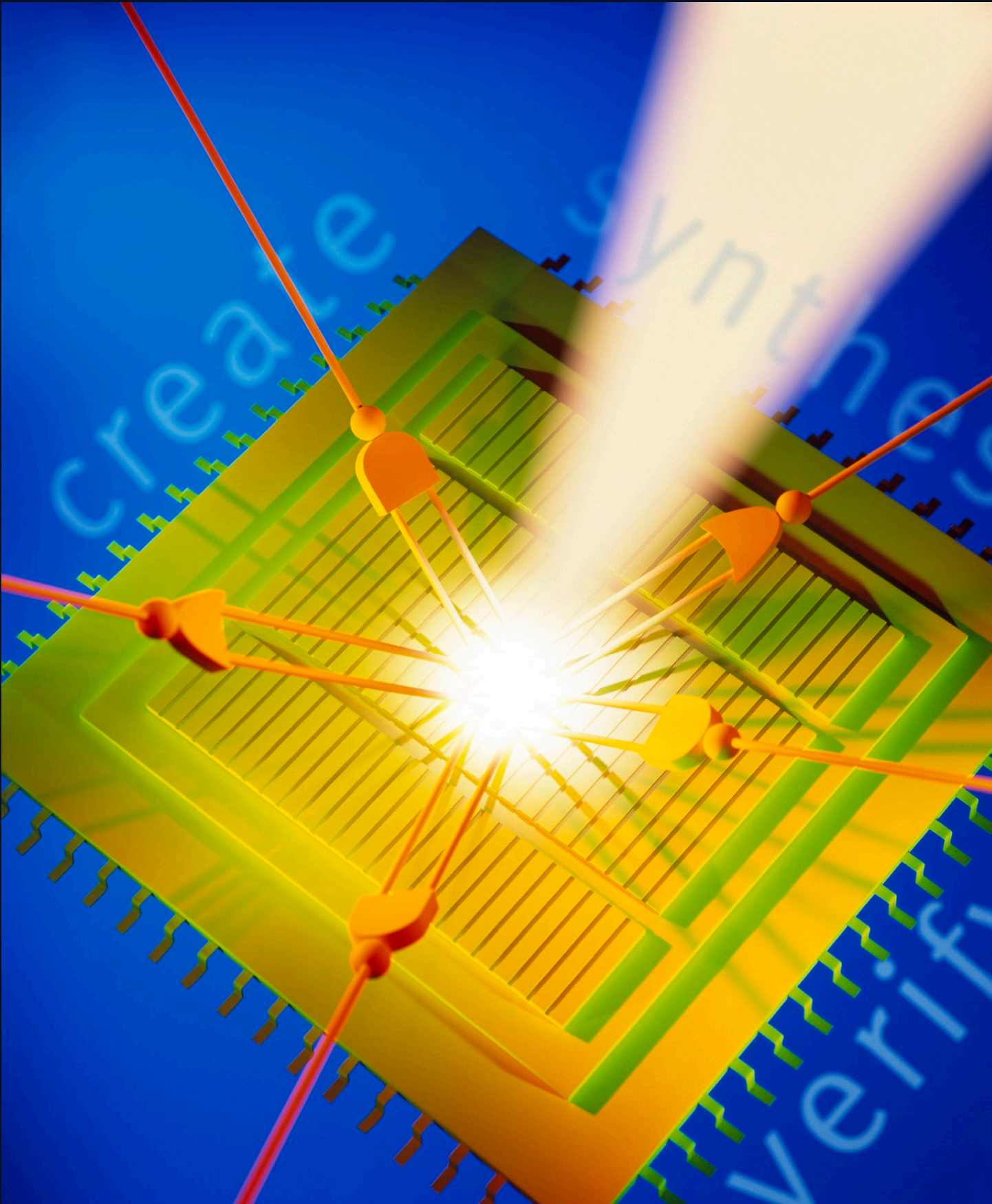


Precision Synthesis

Excellence in FPGA Synthesis



“Supporting FPGA design flows is strategic for Mentor Graphics—we are the only company offering a complete FPGA solution from design entry and simulation to synthesis and PCB design. FPGA synthesis is at the center of our solution. Mentor is fully committed to leadership in FPGA synthesis.”



Walden C. Rhines
Chairman and CEO
Mentor Graphics Corporation

The Need for Advanced FPGA Synthesis

Advanced FPGAs have become vehicles for delivering sophisticated digital technology to service ever broadening applications. With these complex devices come the design challenges of balancing device performance versus area, effectively analyzing and debugging the design to ensure full chip verification, and reaching your market window on time. To ensure the best return on your development investment, you need an FPGA synthesis design tool that can successfully manage design complexity, reduce design risk throughout the project development cycle, increase designer productivity, and protect your negotiation power with FPGA vendors. Mentor Graphics' Precision® Synthesis products provide these crucial benefits to enable you to win in your market.

FPGA Vendor Independence

Precision Synthesis is a vendor-independent FPGA synthesis solution encouraging generic, non-vendor-specific design practices. Through sophisticated design inferencing of FPGA-vendor-neutral HDL, Precision Synthesis optimizes the design for the target device technology, mapping the HDL to the specific resources available in the targeted device, thus removing the burden from the designer to instantiate FPGA-vendor-specific resources. This FPGA-vendor-independent coding frees the designer to select the best FPGA architecture at the best unit cost for each design project and generation.

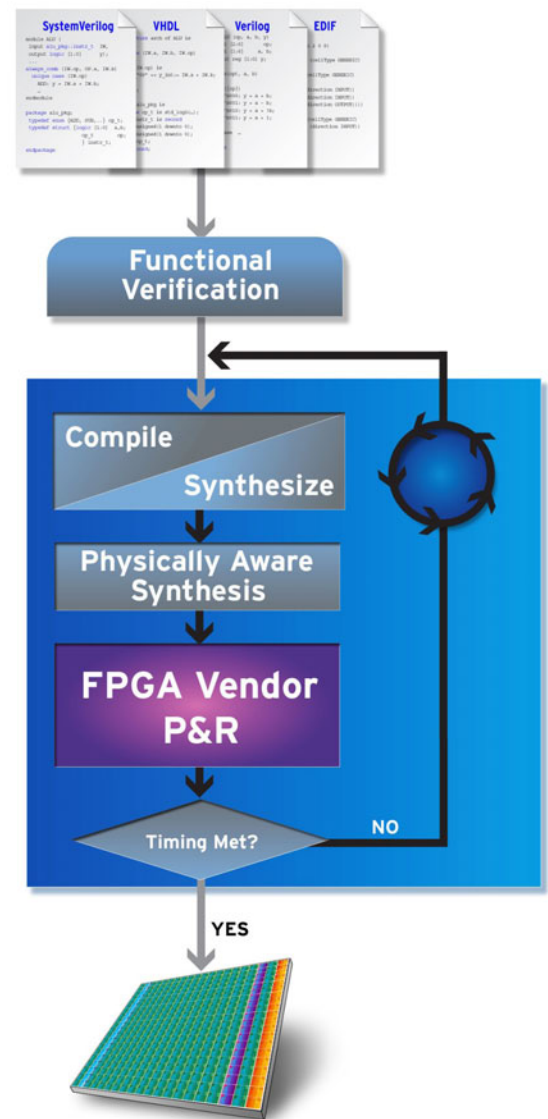
Best-in-Class Language Support

The flexibility to leverage the latest in hardware description languages and use IP from any source requires a tool that delivers HDL freedom. Mentor Graphics consistently delivers the best HDL coverage by supporting SystemVerilog, Verilog, VHDL, EDIF, or any combination of these languages in every Precision product offering.

Precision Synthesis' industry-leading SystemVerilog competence is gaining wide acceptance for both FPGA production designs and ASIC prototyping applications. In addition, our support for the industry-standard Synopsys® Design Constraint (SDC) format strengthens design portability between FPGAs and ASICs.

Physically Aware Synthesis

Physically aware synthesis enables designers to reach their timing goals faster, and with fewer iterations. A push-button, timing-driven methodology, Precision physically aware synthesis provides an optimized netlist to the FPGA vendors' place-and-route tools. This methodology performs pre-place-and-route physical synthesis optimizations based on advanced delay estimation, and considers many factors including potential placement, available routing resources, and design rules specific to each device. Internal and customer testing shows a typical performance improvement ranging from 5 to 40%, with an average improvement of 10%. With 19 FPGA device families and counting, Precision physically aware synthesis provides the industry's broadest support for physical synthesis.



Adding the physically aware synthesis step to the FPGA flow allows designers to reach their timing goals faster with fewer iterations.

Automatic Incremental Synthesis

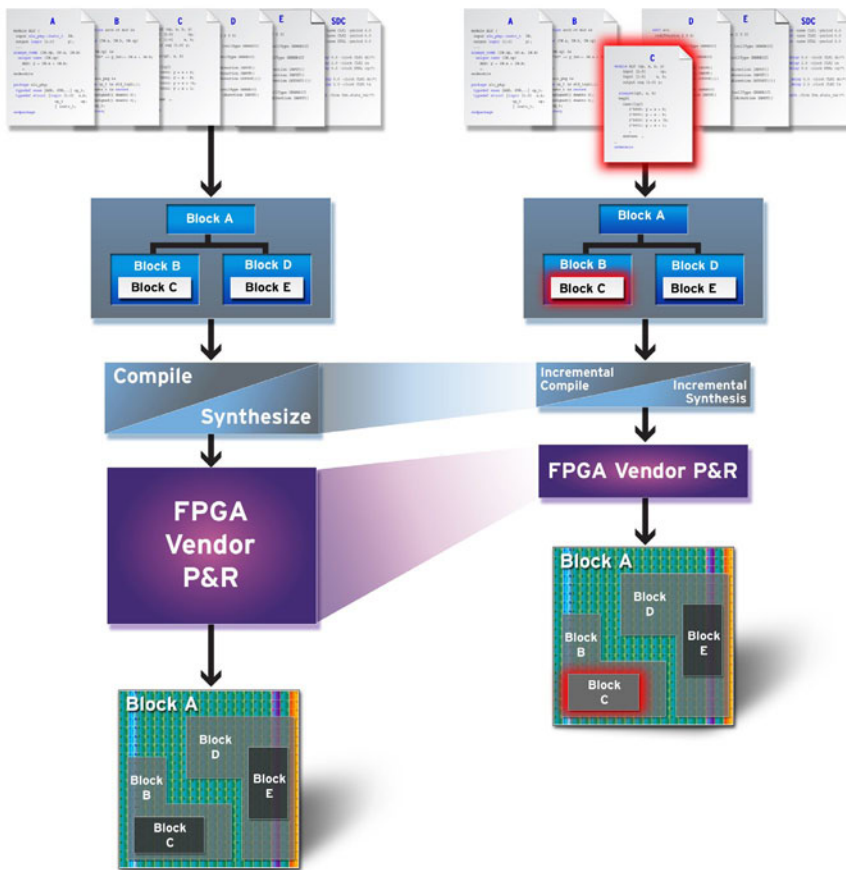
The industry's only automatic incremental synthesis enables any designer to minimize the impact of a late-cycle design change while maintaining the QoR of prior work. Delivering up to 60% runtime improvement without the need for any prior planning or setup, Precision automatic incremental synthesis supports a wide range of FPGA families.

The combination of this new automatic incremental synthesis and the Xilinx SmartGuide flow is the industry's first complete, automatic incremental design flow allowing incremental changes all the way through place and route.

Partition-Based Incremental Synthesis

Precision Synthesis also supports the more typical partition-based incremental synthesis approach supported by Altera and Xilinx. This approach can result in a six-fold improvement in run times and maximize predictability after a design change when compared to traditional synthesis methodologies. Moreover, Precision Synthesis takes partition-based design one step further with technology allowing designers to recompile and synthesize only the sub-portions of the

partition affected by the design change — not only reducing the design iteration loop further, but also preserving even more of the previous design work.

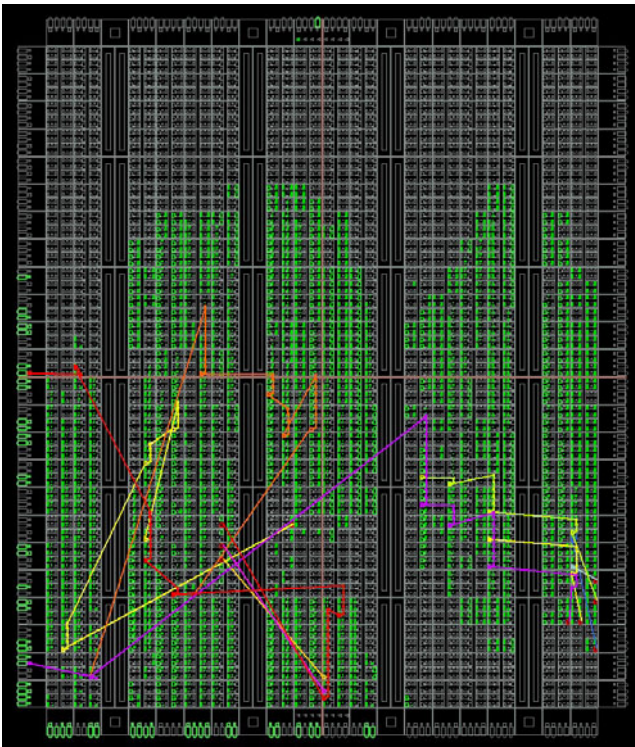


The Precision partition-based incremental synthesis takes traditional block-based iteration one step further by localizing design changes within a partition.

Advanced Optimization

In addition to the advanced optimization capability delivered by physically aware synthesis, Precision synthesizes designs efficiently by automatically inferring memory and DSP functions and mapping them to device-specific blocks, significantly improving area and performance for all advanced FPGA architectures.

High-level optimizations, such as register retiming and physical resource sharing improve the resulting Fmax. Advanced user controls facilitate the investigation of area and performance trade-offs by allowing the user to specifying the desired state machine style and I/O mapping, all resulting in better device utilization and improved performance.



PreciseView displays critical paths and available device real estate.

Resource Manager

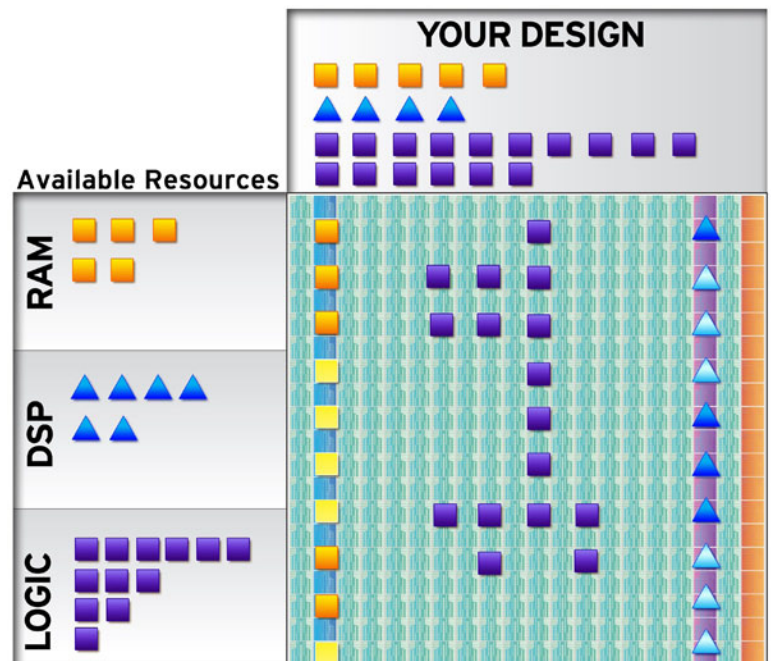
The industry's first resource management technology found in Precision Synthesis enables the engineer to easily make trade-offs to optimize the design for either performance or area by analyzing and manipulating the mapping of dedicated FPGA resources. The tool offers an intuitive interface, allowing the user to easily identify available architectural blocks and re-map implementations for the best performance and device utilization.

Physical Synthesis

Precision Physical combines the logical, timing, and physical worlds into a single intuitive design and analysis environment, enabling designers to take control of their design implementation and timing challenges. The tool enables advanced post-place-and-route physical synthesis based on timing numbers received from the vendor place and route while PreciseView provides a graphical view of the device.

Designers can cross-probe between the timing report, RTL source, RTL schematic and physical view to quickly and accurately identify performance bottlenecks, as well as potential functional issues in the design. Timing problems can then be fixed by either modifying the RTL code or optimizing the cell placements in PreciseView.

The tool also supports engineering change orders (ECO) by allowing designers to preserve the placement (and thus, the performance) of large portions of the design while integrating the changed logic, minimizing both the cost and risks of ECOs.

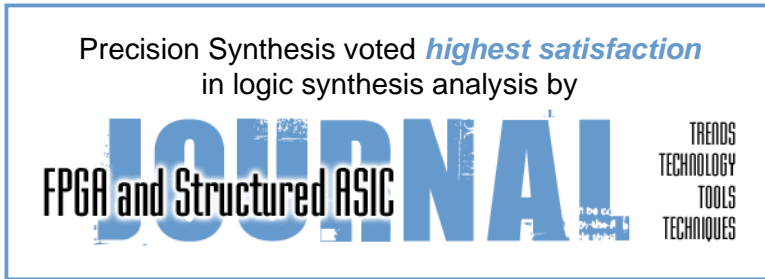


Patent-applied-for resource management technology identifies available architectural blocks and easily enables re-mapping of implementations for best performance and device utilization.

Award-Winning Analysis

Voted as having the highest user satisfaction in logic synthesis analysis by *FPGA and Structured ASIC Journal* due to its powerful integrated timing and design analysis, Precision Synthesis empowers the designer to rapidly identify and isolate logic, timing and constraint issues. Cross-probing between gate-level and the RTL domain, tracing RTL to HDL,

and viewing and tracing critical paths in fragmented path and gate-level technology views permit the user to analyze and explore the design at all levels. Constraint and clock domain analysis is equally important at this level of design complexity to report missing constraints, set proper constraints and I/O delays, and report on signals crossing clock domains.



ASIC Prototyping

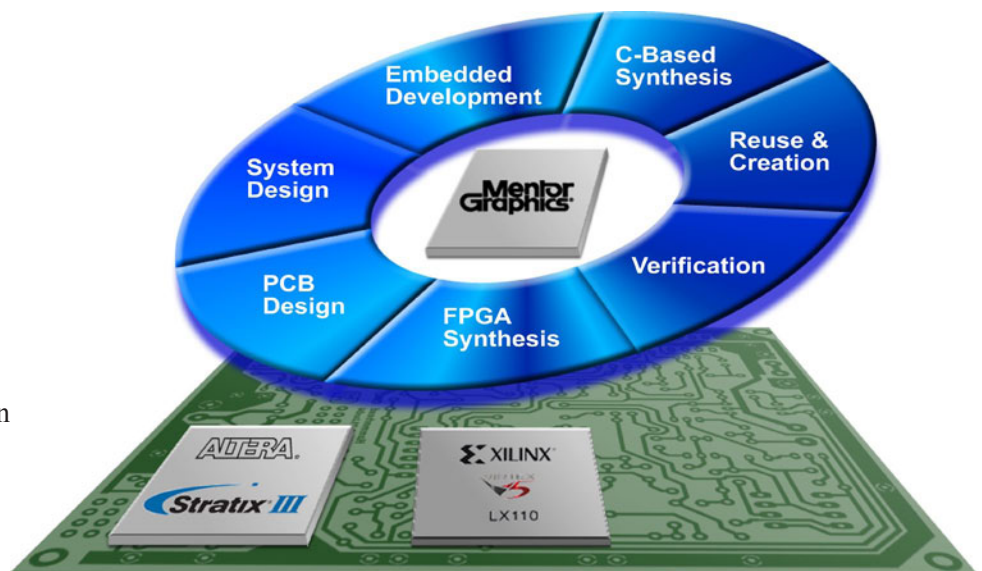
Precision Synthesis delivers advanced support for ASIC prototyping, a crucial step in large-ASIC verification. Support for Synopsys DesignWare® libraries and design constraints (SDC) enable the same design source and constraints to be used for both the ASIC and FPGA targets. Automatic gated-clock conversion throughout the design hierarchy for latches, shift registers, RAM, block multipliers and DSP blocks further aid in a smooth transition between the ASIC and FPGA implementations of the design.

Part of the Mentor Graphics FPGA Design Flow

Precision Synthesis is part of the complete Mentor Graphics FPGA design flow from concept to PCB implementation:

- Electronic System Level (ESL) design with Catapult™ high-level synthesis
- Design analysis, creation and management with HDL Designer Series™ tool suite
- Verification with Questa™ and ModelSim® simulation
- Formal verification with FormalPro™ equivalence checking
- FPGA-on-board design with I/O Designer™ flow integration

Mentor Graphics has the industry's most comprehensive FPGA design tools and solutions.



The Precision Family of Synthesis Products

Precision Synthesis products are the most advanced synthesis tools available for FPGA design. Precision RTL Synthesis offers FPGA-vendor-independence, industry-leading hardware language and constraint support, advanced optimizations, and award-winning analysis and debug. Precision RTL Plus Synthesis adds improved productivity with physically aware synthesis, incremental synthesis flows, and resource management. Precision Physical Synthesis completes the offering by adding post-place-and-route physical optimizations and the PreciseView graphical viewer and editor. Precision Synthesis helps designers maximize the potential of their designs.

FEATURES	Precision® RTL	Precision® RTL Plus	Precision® Physical
Advanced Optimization Algorithms	✓	✓	✓
RTL & Technology Schematic Viewers	✓	✓	✓
Vendor Independence	✓	✓	✓
Interactive Static Timing Analysis	✓	✓	✓
Gated Clock Conversions	✓	✓	✓
DSP & RAM Inference Optimization	✓	✓	✓
SystemVerilog Support	✓	✓	✓
Register Retiming	✓	✓	✓
Physically Aware Synthesis		✓	✓
Incremental Design Flows		✓	✓
Resource Manager		✓	✓
Advanced Physical Synthesis			✓
PreciseView Debug			✓
Placement Reuse/ECO			✓

To learn how Precision Synthesis can address your FPGA design needs, call Mentor Graphics to schedule a product demonstration, or visit our website for the latest product news and information at www.mentor.com/synthesis.

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Corporate Headquarters
Mentor Graphics Corporation
8005 SW Boeckman Road
Wilsonville, OR 97070-7777
Phone: 503.685.7000
Fax: 503.685.1204

Sales and Product Information
Phone: 800.547.3000

Silicon Valley
Mentor Graphics Corporation
1001 Ridder Park Drive
San Jose, California 95131 USA
Phone: 408.436.1500
Fax: 408.436.1501

North American Support Center
Phone: 800.547.4303

Europe
Mentor Graphics
Deutschland GmbH
Arnulfstrasse 201
80634 Munich
Germany
Phone: +49.89.57096.0
Fax: +49.89.57096.400

Pacific Rim
Mentor Graphics (Taiwan)
Room 1001, 10F
International Trade Building
No. 333, Section 1, Keelung Road
Taipei, Taiwan, ROC
Phone: 886.2.87252000
Fax: 886.2.27576027

Japan
Mentor Graphics Japan Co., Ltd.
Gotenyama Hills
7-35, Kita-Shinagawa 4-chome
Shinagawa-Ku, Tokyo 140
Japan
Phone: 81.3.5488.3033
Fax: 81.3.5488.3004

